Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to overcome Examiners Section 112 rejections and to correct a grammatical errors and to clarify Applicants invention.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

For example support for the amendments are found in the Figures, the original claims and the Specification, for example beginning at paragraph 0018:

"Referring to Figure 1D, following photolithographic patterning (photoresist layer not shown), in a first step of the multi-step RIE etching process, the hardmask layer is etched through a thickness using a CF_4 etching chemistry to expose portions of the underlying polysilicon layer 18 leaving hardmask layer portions e.g., 20A and 20B overlying subsequently formed polysilicon gate electrode portions."

And at paragraph 0020:

"Referring to Figure 1F, a second main etch step is then carried out where the polysilicon layer 18 is etched through a second thickness portion, for example in one embodiment **to endpoint detection of an underlying gate dielectric layer 16 to at least partially expose the underlying gate dielectric layer.** In the second main etch step, at least the RF bias power and preferably both the RF bias power and the RF source power are reduced compared to the first main etch step."

And at paragraph 0025:

"Referring to Figure 1G, following the inert gas plasma treatment, an **overetch process is carried out to remove remaining portions of the polysilicon layer** 18 over the gate dielectric layer 16 including removing polysilicon stringers."

Claim Rejections under 35 USC 112

Applicants have amended claims 1, 14, and claims 9 and 19 to overcome Examiners rejections.

Claim Rejections under 35 USC 103

Claims 1, 2, 4-9, 11-12, 14-19, and 21-22 stand rejected under 35 USC 103(a) as being unpatentable over Lee (5,665,203 in view of Pan et al. (US 6,656,832).

Statement of Common Ownership Pursuant to 35 USC 103(c)

Applicants attorney of record state that Pan et al. (US 6,656,832) and Applicants instant application were, at the time the invention was made, owned by Taiwan Semiconductor Manufacturing Company. Therefore, Examiners use of Pan et al. as a reference in a 103(a) rejection appears to be improper under 35 USC §103(C).

However, while not agreeing US 6,656,832 may be properly be used as a reference in a rejection under 103(a), assuming *arguendo* that it is a properly used reference, Applicants respectfully traverse Examiner's rejection under 35 U.S.C. 103(a).

Lee discloses a method for reactive ion etching of a gate electrode using an oxide hardmask layer and a three step silicon

etching process. Lee et al. disclose in a first chamber etching with CF4 to remove any oxide that may have formed on the polysilicon layer during stripping of the resist mask (col 4, lines 31-35). After transfer to a silicon etching chamber a second step is carried out using HBR/CL2/O2 in a first silicon etching step (second etching step)(col4, lines 34-36) and then HBR/O2 in a third etching step(second silicon etching step)(col 4, lines 52-67).

Lee overcomes the problem of etching polysilicon gates to obtain vertical sidewalls (see col 1, lines 5-9) by oxidizing the sidewalls of the silicon during the first silicon etch step (second etch step) (col 1, lines 63-66; col 4, lines 38-46) and **stopping a predetermined distance (20 nm) above the gate oxide layer (without exposing the gate oxide), then** removing substantially all CL2 from the etching chamber atmosphere (col 2, lines 1-5; col 4, lines 47-51), and **then etching through a remaining thickness portion of the silicon layer to expose the gate oxide layer** (col 2, lines 1-5; col 4, lines 52-64) where the second silicon etch step (third etch step) includes an overetch process. Lee discloses using low pressure and low power density in the second silicon etch step to expose the gate oxide layer with **no magnetic field enhancement** (col 4, lines 64- col 5, line

3).

Lee does not disclose or suggest performing a plasma treatment following exposure of portions of an underlying gate dielectric.

On the other hand, Pan et al. discloses a plasma treatment process using **argon and/or hydrogen** for **treating a via opening** prior to filling the via with a conductor (see Abstract). Pan et al. disclose that **preferably a hydrogen plasma treatment precedes an argon plasma treatment** (col 6, lines 28-31) as well as teaching a high (e.g., preferably greater than 600Watts) and a high bias power (e.g., preferably greater than 450 Watts) (col 6, lines 22-28). Pan et al. teach that the high power and bias power in the hydrogen plasma treatment, together with the low RF power and low bias poser in the argon treatment **is useful for cleaning the conductor contact region** in the via, particularly **cleaning copper oxide** (col 6, lines 54-62).

There is no apparent motivation for combining the disparate teachings of Pan et al., who teach a plasma treatment process for **cleaning a via with a hydrogen plasma at high power and bias** with the **gate electrode etching process of Lee who teaches a low power**

etching step (which includes overetching) to expose an underlying gate oxide to avoid damage to the gate oxide, and who **does not suggest or disclose an intervening plasma treatment step (between polysilicon etch and overetch step)**. Moreover, the plasma treatment process of Pan et al. would likely damage the device of Lee including the gate dielectric of Lee.

Even assuming *arguendo*, a proper motivation for the combination the plasma treatment including **hydrogen plasma** of Pan et al. with the teaching of Lee et al., such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).*

2. Claims 3, 10, 13, 20, and 23 stand rejected over Lee and Pan et al., above, and further in view of Lill et al. (US 6, 284,665).

Applicants reiterate the comments made above, with respect to Lee and Pan et al.

Applicants disagree with Examiners assertion that self-bias is equivalent to zero bias power, and Examiners discussion of Lill et al. refutes such an assertion. Lee discloses the use of a **low bias voltage** in the range of 50 to 100 Volts to avoid ion damage to the gate oxide layer (col 2, lines 46-49) in a polysilicon etchback (planarization etching) process with an underlying silicon nitride layer.

The fact that Lill et al. teaches typical process condition for RIE of polysilicon selectively to silicon nitride in a polysilicon etchback (flat etch front) process including the use of a low bias Voltage, does not further help Examiner in establishing a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining

the disparate teachings of plasma process conditions for a polysilicon etchback process (Lill et al.) with a plasma cleaning treatment to remove copper oxide within a via (Pan et al.) with a polysilicon gate etch process (Lee) where an inert plasma treatment is neither suggested or disclosed, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).*

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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